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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/721,086	11/26/2003	Hirofumi Shibuya	XA-9985	7814

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MILES & STOCKBRIDGE PC
1751 PINNACLE DRIVE
SUITE 500
MCLEAN, VA 22102-3833

EXAMINER	
KIM, DANIEL Y	

ART UNIT	PAPER NUMBER
2185	

DATE MAILED: 05/31/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/721,086	SHIBUYA ET AL.	
	Examiner	Art Unit	
	Daniel Kim	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 April 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This Office Action is in response to applicant's communication filed April 4, 2006 in response to the PTO Office Action mailed January 4, 2006. The applicant's remarks and amendments to the claims and/or the specification were considered with the results that follow.

2. In response to the last Office Action, claims 1-2, 7-8 and 10 have been amended, and no other claims have been canceled or added. Claims 1-10 remain pending in this application.

3. The objections to claim 1 has been withdrawn due to the amendment filed April 4, 2006.

Response to Arguments

4. Applicant's arguments with respect to claims 1-10 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1-5 are rejected rejected under 35 U.S.C. 102(e) as being anticipated by Thelin et al (US Patent No. 7,024,614).

For claim 1, Thelin discloses a storage device comprising one or more semiconductor memories and an information processing section which performs a first operation for reading data stored in the one or more semiconductor memories and a seconds operation for writing data to the one or more semiconductor memories in accordance with commands received from outside thereof (a field read/write module which handles reading and writing system files located in a reserved area of a disk or in semiconductor memory, col. 11, lines 44-46),

wherein the information processing section detects an error state associated with an area in the semiconductor memory (an error recovery module is invoked by a check disk module and implements various error recovery techniques, including retry error recovery and firmware error correction code processing when an error is detected while accessing the disk, col. 11, lines 57-62; a plurality of state queues, wherein each queue stores a number of segment descriptors having a particular allocation state such as free, valid, dirty, etc., as well as a write verify queue which stores segment descriptors implementing write commands waiting to be verified through a write verify operation,

and the write verify operation reads recently written data sectors to verify recoverability, and may fail relative to a configurable error recovery threshold, col. 10, lines 7-14),

substitutes the area during an idle state, where operations are not being performed in response to the commands, when the error state is indicated to be a critical state (the write verify operation is performed by the background task when the disk drive is idle and not processing host commands, col. 10, lines 7-17), and'

substitutes the area immediately when the error state is indicated to be a limit state (an auto-relocation module relocates data blocks from marginal data sectors detected during a write verify operation to spare data sectors, col. 11, lines 47-51).

Claim 2 is rejected using the same rationale as for the rejection of claim 1 above.

For claim 3, Thelin discloses independently setting the factors for the information processing section to determine a critical state and setting the factors for the information processing section to determine a limit state (the disk drive comprises an error recovery system, wherein the configuration parameters configure the error recovery system or the read/write channel, col. 2, lines 25-28).

For claim 4, Thelin discloses a substitution destination area substituted by the information processing section is a free area in the semiconductor memory or semiconductor memory for substitution only (if the number of write verify failures exceeds a threshold, the data block stored in the marginal data sector associated with the segment descriptor is relocated to a spare data sector, col. 8, lines 10-12).

For claim 5, Thelin discloses the substitution destination area is a free area in the semiconductor memory, the substitution destination area is a physical area controlled

by an individual peripheral circuit which controls any of a plurality of sectors provided for a memory mat (a microprocessor for executing disk commands by initializing configuration data structures comprising a plurality of configuration parameters with predetermined default values, col. 2, lines 11-14).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Thelin et al (US Patent No. 7,024,614) and Harari et al (US Patent No. 5,991,517).

For claim 6, Thelin discloses the invention as per rejection of claim 5 above.

Thelin fails to disclose the limitations of the current claim.

Harari, however, helps disclose a decode method of the device substitutes only data in a substitution origin area for data in a substitution in a substitution destination area, after substitution, allows access to the substitution destination area instead of the substituted area, and allows access to an unsubstituted area in the same manner as before the substitution (when the controller is given an address to access data, the controller compares this address against the sector defect map. If a match occurs then access to the defective sector is denied and the substitute address present in the defect map is entered, and the corresponding substitute sector is accessed instead. The sector

remapping is performed by a microprocessor. The microprocessor looks at the incoming address and compares it against the sector defect map. If a match occurs, it does not issue the command to the controller but instead substitutes the alternative location as the new command, col. 14, lines 14-25).

Thelin and Harari are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory management. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include substitution of data and allow access to the substitution destination area instead of the substituted area because this would enable error correction codes to adequately rectify errors that may crop up in the system (col. 2, lines 39-43), as taught by Harari.

9. Claims 7-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Thelin et al (US Patent No. 7,024,614) and Schwarz (US Patent No. 6,496,947).

For claim 7, Thelin discloses the invention as per rejection of claim 1 above.

Thelin fails to disclose the limitations of the current claim.

Schwarz, however, helps disclose the information processing section notifies an outside of an emergency condition (with each read, a compare circuit compares the actual data read from a cell with expected data and notifies a BIST circuit of any errors, col. 6, lines 65-67, col. 7, line 1).

Thelin and Schwarz are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory management. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include

notifying an outside of an emergency condition because this would then allow errors to be repaired through said address re-mapping or other procedures (col. 7, lines 1-5), as taught by Schwarz.

For claim 8, the combined teachings of Thelin and Schwarz disclose the invention as per rejection of claim 7 above.

Schwarz further helps disclose one or more restricting operations, including inhibiting a write operation (a built-in test circuit coupled to the memory array for executing a sequence of write and read operations on the memory array, and a pause circuit coupled to and activated by the built-in self test means for pausing the sequence of read and write operations, col. 2, lines 30-34).

For claim 9, the combined teachings of Thelin and Schwarz disclose the invention as per rejection of claim 8 above.

Schwarz further helps disclose correcting of a correctable error if it is contained in the data (a compare circuit which compares actual data read from the cell with the expected data and notifies a testing circuit of any errors, which are either repaired through address re-mapping circuit or, if the error cannot be repaired, the testing circuit activates a fail flag, col. 6, lines 66-67 and col. 7, lines 1-5).

Claim 10 is rejected using the same rationale as for the rejections of claims 1, 6, 7 and 8 above.

Contact Information

10. Any inquiries concerning this action or earlier actions from the examiner should be directed to Daniel Kim, reachable at 571-272-2742, on Mon-Fri from 8:30am-5pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan, is also reachable at 571-272-4210.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information from published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. All questions regarding access to the Private PAIR system should be directed to the Electronic Business Center (EBC), reachable at 866-217-9197.

DK

5-26-06

PIERRE VITAL
PRIMARY EXAMINER